APPLICATION

FOR

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TITLE: **COMBINING FREQUENCY MULTIPLICATION WITH MODULATION**

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COMBINING FREQUENCY MULTIPLICATION AND MODULATION

BACKGROUND

The invention generally relates to combining frequency multiplication and modulation (linear modulation, for example).

The generation of high frequency carrier signals (microwave carrier signals, for
5   example) for use in communication systems (wireless communication systems, for example) presents challenges. For example, the implementations of microwave voltage controlled oscillators (VCOs) in integrated circuits makes its increasingly difficult to make these VCOs stable and able to produce clean carrier signals, especially in view of the trend to make these VCOs operate at ever-increasing frequencies. Furthermore, it is more difficult to design the
10   phase locked loops of these VCOs for such high frequencies.

For these reasons, a modulation system 10 that is depicted in Fig. 1 may be used. In the system 10, a local oscillator 12 (a VCO, for example) generates a signal (a sinusoidal signal, for example) that has a fundamental frequency that is a fraction (one third, for example) of the frequency of the carrier signal. This signal from the oscillator 12 is received
15   by a frequency multiplier 14 that multiplies (multiplies by three, for example) the frequency of this signal to produce the carrier signal, a signal that has a fundamental frequency that is three times the fundamental frequency of the signal from the oscillator 12. This carrier signal may be used by a modulator 16 to modulate an input signal at the carrier frequency to produce a modulated signal. Thus, the design of the oscillator 12 is simplified due to its
20   lower frequency of operation, as compared to an oscillator that directly generates the carrier signal.

However, a difficulty with the modulation system 10 is that the frequency multiplier 14 may introduce a significant amount of spectral energy into the carrier signal at frequencies other than the carrier frequency. This distortion of the carrier signal may, in turn, expand or
25   distort the modulated signal. Although it may be possible to pre-distort the original modulation to compensate for the distortion that is introduced by the frequency multiplier 14, this pre-distortion may not always be desirable for various reasons.

Thus, there is a continuing need for a technique and/or arrangement to address one or more of the problems that are stated above.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a schematic diagram of a modulation system of the prior art.

Fig. 2 is a schematic diagram of a modulation system according to an embodiment of the invention.

Fig. 3 is a schematic diagram of a modulator of Fig. 2 according to an embodiment of the invention.

Fig. 4 is a schematic diagram of a transmitter according to an embodiment of the invention.

DETAILED DESCRIPTION

Referring to Fig. 2, an embodiment 50 of a modulation system in accordance with the invention includes an modulator 62 that modulates a complex input signal to produce a modulated signal (called S2) at output terminals 72 of the system 50. The modulator 62 may, for example, be a linear modulator that linearly modulates the amplitude of the input signal pursuant to a Quadrature Amplitude Modulation (QAM) technique (for example).

The S2 signal indicates the modulation of the input signal at a carrier frequency. However, unlike a conventional modulation system, the modulator 62 does not modulate the input signal with a signal that cycles at the carrier frequency. Instead, the modulator 62 includes a multiplier 63 (described in more detail below) to modulate the input signal with phase shifted carrier signals (called M1 and M2) that each have a fundamental frequency that is a fraction of the carrier frequency of the S2 signal. The M1 and M2 signals are produced by a local oscillator 52 that operates at the fundamental frequency of the M1, M2 signal. In some embodiments of the invention, the modulation by the multiplier 63 produces a modulated signal (called S1 and appearing at the output terminals 68 of the multiplier 63) that has a carrier frequency that is near the fundamental frequency of the M1, M2 signal.

Thus, the carrier frequency of the S1 signal (and the frequency of operation of the oscillator 52) is a fraction of the carrier frequency of the S2 signal. However, the oscillator 52 is permitted to operate at this lower frequency due to the frequency multiplication that

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occurs when the multiplier 63 modulates the input signal with the M1 and M2 signals. In this manner, the modulation by the multiplier 63 produces spectral components (in the S1 signal) that are located at, for example, odd multiples (three times, five times, seven times, etc.) of the fundamental frequency of the M1, M2 signal. These higher frequencies that are multiples of the fundamental frequency of the M1, M2 signal are called harmonics, and the spectral energy near each one of these harmonics indicates the modulation of the input signal at the particular harmonic.

Therefore, for purposes of producing the S2 signal, the modulation system 50 includes a bandpass filter (BPF) 70 that is coupled to the multiplier 63 to tune the modulation to the selected harmonic to produce the desired carrier frequency of the S2 signal. To accomplish this, the BPF 70 has a passband that is centered near a selected one of the harmonics, and the BPF 70 has appropriate rolloff characteristics to create a stopband to reject spectral components (of the S1 signal) that are located at the carrier frequency of the S1 signal and to reject other harmonics present in the S1 signal. This filtering produces the S2 signal that includes substantially more spectral energy near the selected harmonic than near the fundamental frequency of the M1, M2 signal. Thus, the S2 signal indicates the modulation of the input signal at the carrier frequency, although this carrier frequency is significantly higher than the frequency of operation of the oscillator 52.

Due to the combined modulation and frequency multiplication of the modulator 62, the oscillator 52 does not operate at the carrier frequency of the S2 signal, thereby simplifying the design of the oscillator 52. Furthermore, no explicit frequency multiplier is used.

As depicted in Fig. 2, the S1 and S2 signals are separate signals in some embodiments of the invention. However, as described in another embodiment below, the BPF 70 is coupled to the multiplier 63 to tune the modulation so that the multiplier 63 furnishes the S2 signal at its output terminals. Thus, in these embodiments, the S2 signal is directly provided by the multiplier 63 without generation of the S1 signal.

As a more specific example, in some embodiments of the invention, the M1 and M2 signals may be sinusoidal signals, and the fundamental frequency of the M1, M2 signal may be one third of the carrier frequency of the S2 signal. The BPF 70 may have a passband that passes the spectral energy of the S1 signal that is associated with the third harmonic of the S1 signal to produce the S2 signal, a signal that has a carrier frequency that is three times that of

the fundamental frequency of the M1, M2 signal. Thus, the filtering by the BPF 70 in this example produces an S2 signal that includes substantially more spectral energy near the third harmonic of the fundamental frequency of the M1, M2 signal than near the fundamental frequency or near other harmonics.

5   The M1 and M2 signals may be provided by a 90° phase shifter 56 that receives a sinusoidal (for example) signal from an output terminal 54 of the oscillator 52. The phase shifter 56 passes through the sinusoidal signal from the oscillator 52 to produce the M1 signal at an output terminal 58 of the phase shifter 56. The phase shifter 56 also shifts the sinusoidal signal received from the oscillator 52 by 90° to produce the M2 signal. Thus, the

10   M1 and M2 signals have the same fundamental frequency but are shifted apart by 90°. In some embodiments of the invention, the oscillator 52 may be a voltage controlled oscillator (VCO).

The input signal is a complex signal that is formed from a real component that is indicated by an analog signal (called Q) and an imaginary component that is indicated by an

15   analog signal (called I). The I and Q signals are differentially received by input terminals 64 and 66, respectively, of the modulator 62.

Referring to Fig. 3, in some embodiments of the invention, the multiplier 63 may be formed from two Gilbert cell multipliers 100 and 120. The Gilbert cell multiplier 100 multiplies the I signal with the M1 signal, and the Gilbert cell multiplier 120 multiplies the Q

20   signal with the M2 signal. The multipliers 100 and 120 are coupled together to produce, in conjunction with the tuning that is provided by the BPF 70, the S2 signal that appears at the output terminals 72. For the embodiment that is depicted in Fig. 3, the output terminals 68 of the modulator 62 are also the output terminals 72 of the BPF 70.

In the Gilbert cell multiplier 100, the terminals 58 (see Fig. 2) differentially receive

25   the M1 signal. The terminals 64 differentially receive the I signal. One of the terminals 58 controls a transistor 142 that modulates current (from a current source called I_{SS}) through a differential transistor pair 144 that, in turn, is controlled by the I signal. Another one of the terminals 58 controls a transistor 146 that modulates current from the I_{SS} current, which flows through a differential transistor pair 150. The differential transistor pair 150, in turn, is also

30   controlled by the I signal. The output terminals of the differential transistor pairs 144 and 150 are cross coupled together to form output terminals 104 of the Gilbert cell multiplier 100,

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as can be appreciated by one skilled in the art.

In the Gilbert cell multiplier 120, the terminals 60 (see Fig. 2) differentially receive the M2 signal. The terminals 66 differentially receive the Q signal. One of the terminals 60 controls a transistor 130 that modulates current from the I_{SS} current source through a differential transistor pair 132 that, in turn, is controlled by the Q signal. Another one of the terminals 60 controls a transistor 134 that modulates current from the I_{SS} current source, which flows through a differential transistor pair 136. The transistor pair 136, in turn, is also controlled by the Q signal. The output terminals of the differential transistor pairs 132 and 136 are cross-coupled together to form output terminals 124 of the Gilbert cell multiplier 120, as can be appreciated by one skilled in the art.

The output terminals 104 of the Gilbert cell multiplier 100 are formed from the output terminals of the differential transistor pairs 144 and 150. The output terminals 124 of the Gilbert cell multiplier 120 are formed from the differential transistor pairs 132 and 136. The output terminals 104 of the Gilbert cell multiplier 100 are coupled in parallel with the output terminals 124 of the Gilbert cell multiplier 120 to form the output terminals 68 and 72.

Also depicted in more detail in Fig. 3 is an embodiment of the BPF 70. As shown, the BPF 70 may include an inductor 125 and a capacitor 128 that are coupled in parallel between the output terminals 68 and 72. The inductance and capacitance values for these elements are chosen to tune the passband of the BPF 70 to select the desired harmonic to produce the S2 signal.

Fig. 4 depicts an embodiment 300 of a wireless transmitter that uses the modulation system 50. As an example, the transmitter 300 may be an Orthogonal Frequency Division Multiplexing (OFDM) transmitter, although are types of transmitters (wireless and non-wireless) may be used with the modulation system 50 and are within the scope of the appended claims.

During its course of operation, an encoder 312 of the transmitter 300 receives data (via communication lines 311) to be transmitted over a wireless link. The encoder 312 may, for example, introduce an error correcting scheme into the data. The encoder 312 may also perform other operations on the received data, such as a mapping operation, for example. More specifically, the encoder 312 may map the data received by the encoder 312 into a complex value space pursuant to quadrature amplitude modulation (QAM). Other and

different operations by the encoder 312 are possible.

The encoder 312 provides the encoded data (via communication lines 313) to an Inverse Fast Fourier Transform (IFFT) engine 314 of the transmitter 300. The encoded data may be viewed as being divided into segments, with each segment representing a coefficient

5   that is associated with one of a subset of OFDM subcarriers that are assigned to the transmitter 300.

The IFFT engine 314 modulates these coefficients with the assigned subcarriers to produce time-varying digital real and imaginary signals. These digital signals, in turn, are communicated (via communication lines 319) to digital-to-analog converters (DACs) 320

10   that convert these digital signals into the analog I and Q signals that appear on the input terminals 64 and 66 of the modulation system 50. The analog signal that appears at the output terminals 72 of the modulation system 50 is communicated to an antenna interface 330 that drives an antenna 340 with this analog signal.

While the invention has been disclosed with respect to a limited number of

15   embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of the invention.

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